



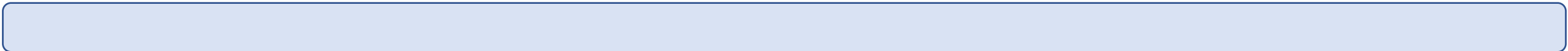
RADIOBLOCKS

Exec Meeting

WP3

Gundolf Wieching (MPIfR)

WP3 Coordinator on behalf of the WP3 RADIOBLOCKS Team





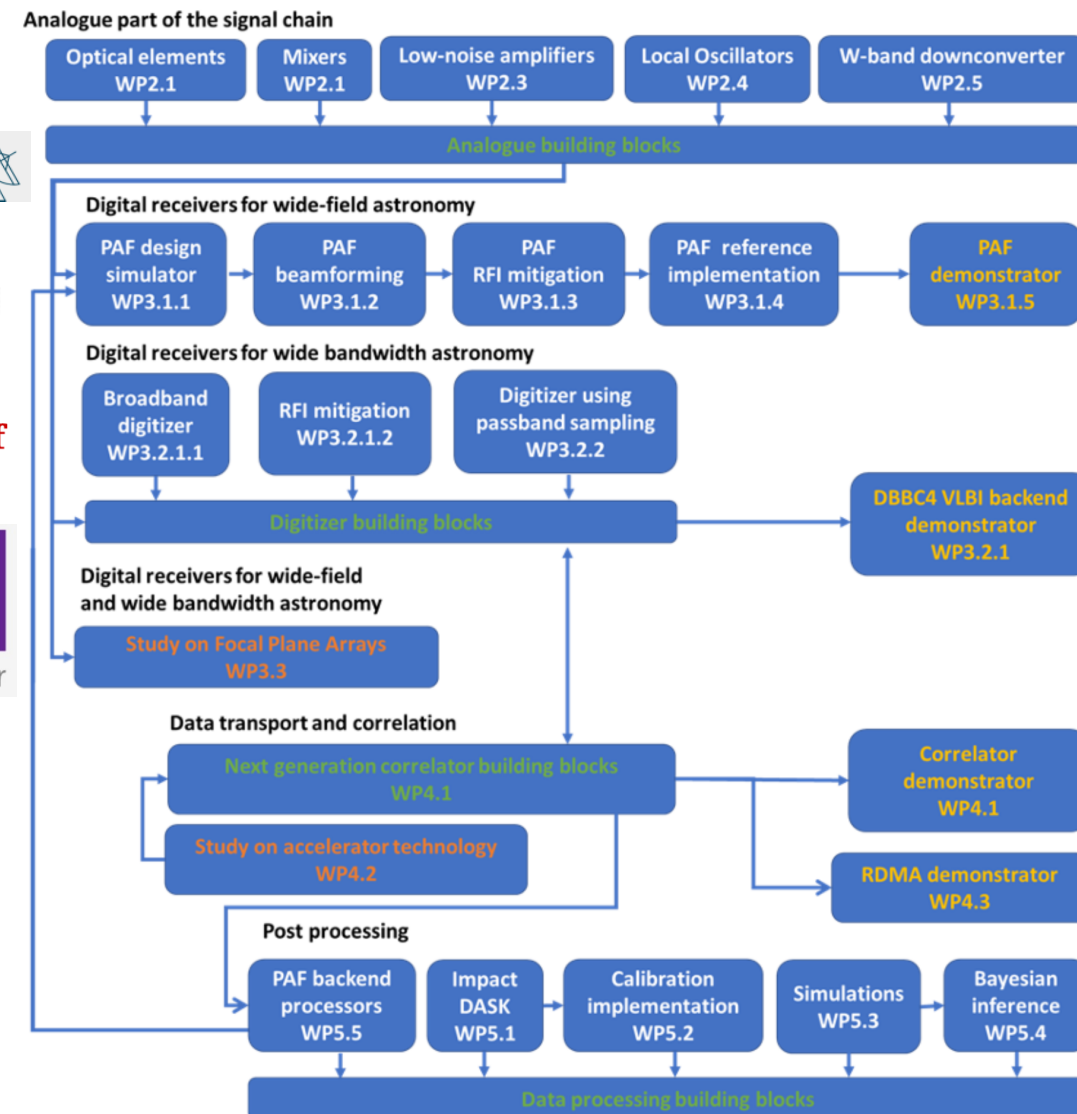
Overview WP3

Partners

- MPG: Max-Planck Institute for Radio Astronomy
- INAF: Istituto Nazionale di Astrofisica
- RUG: Rijksuniversiteit Groningen
- UniMAN: The University of Manchester
- HES-SO: Institut des Technologies de l'Information et de la Communication

Total budget: 1,7M€

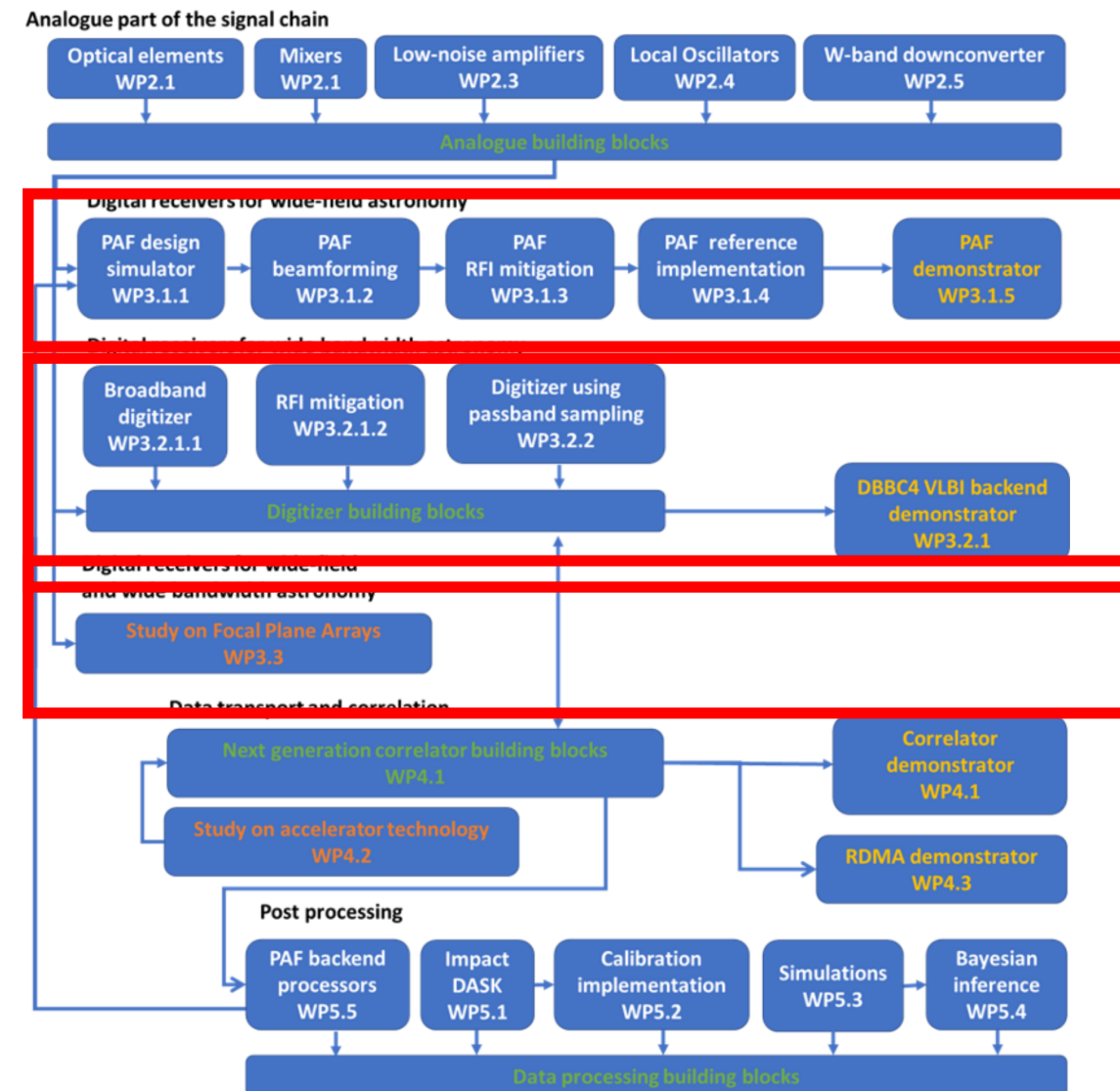
Duration: 4 years (3/2023 - 3/2027)



Overview WP3

- Focus on
 - system temperature (WP3.1)
 - Bandwidth (WP3.2)
 - field-of-view (WP3.1 & WP3.2)
- Provides building blocks to the community
 - Wide filed astronomical receivers WP3.1
 - Wide observation bandwidth WP3.2
 - Study on high frequency multiple pixels systems WP3.3
- Strong interaction between
 - WP2 and WP3.3 on technological feasibilities
 - WP3.1 and WP5.5 on PAF beamforming algorithms

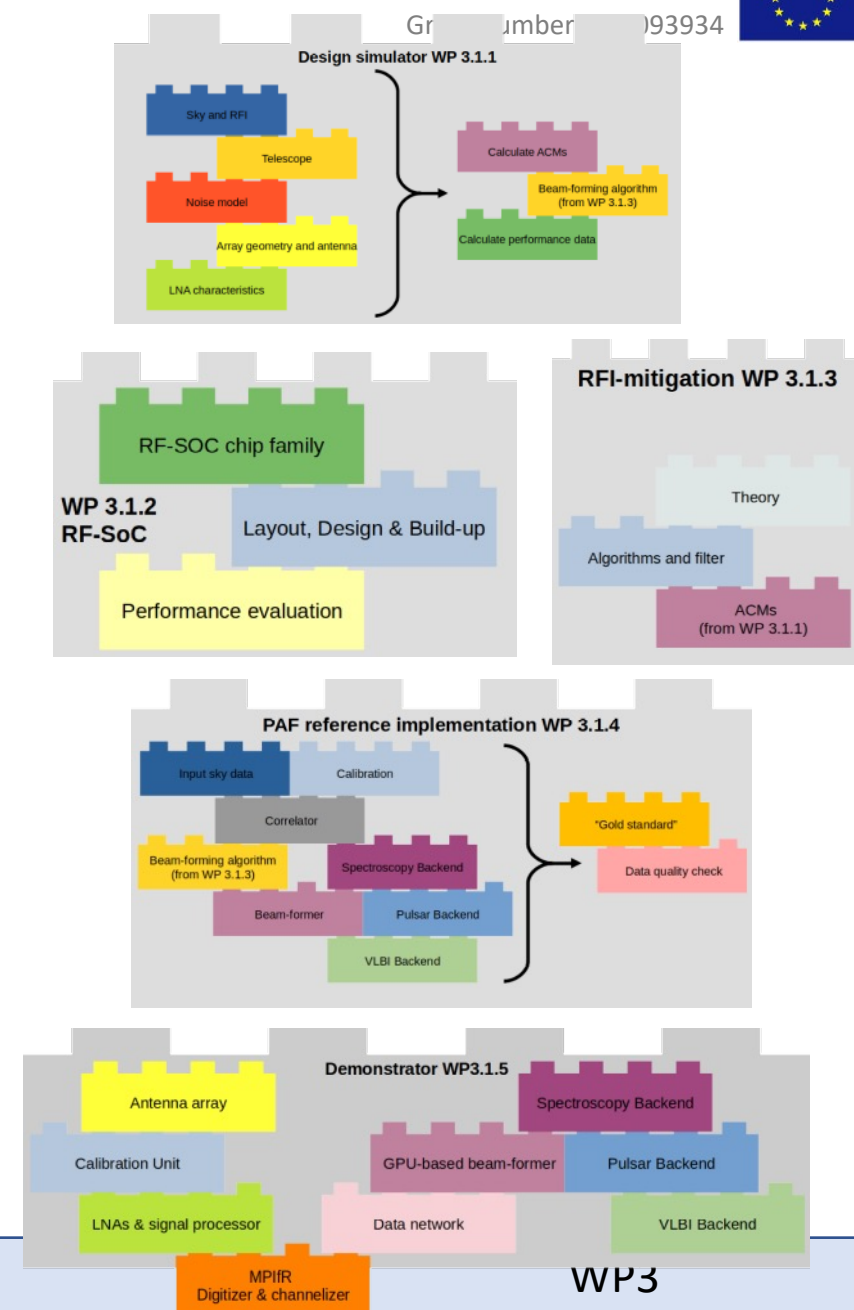
Multiple links to analogue (WP2) and to the digital domain (WP4, WP5)



Structure

WP3 has been structured in tasks and broken down in small blocks

- Task 3.1 Wide field astronomical receivers (Stefan Heyminck)
 - Task 3.1.1: Design Simulator Wide field astronomy ([MPG](#) / INAF / UNIMAN)
 - Task 3.1.2: Novel Beamforming technology on RFSoc ([UNIMAN](#) / INAF / MPG)
 - Task 3.1.3: PAF-RFI mitigation and adaptive beamforming methods ([MPG](#) / INAF / UNIMAN)
 - Task 3.1.4: PAF Reference implementation ([MPG](#) / UNIMAN / INAF)
 - Task 3.1.5: Demonstrator ([MPG](#) / INAF / UNIMAN)
- Task. 3.2 Wide observation bandwidth (Helge Rottmann)
 - Task. 3.2.1 DBBC4 VLBI backend demonstrator
 - Task 3.2.2. DiFrEnd28 and DiFrEnd4T broadband digitizers ([MPG](#) / INAF)
 - Task 3.2.3. RFI-Mitigation: A-EYE Artificial Intelligence Controller ([INAF](#) / MPG)
 - Task 3.2.4 High-frequency digitizing and AI-driven bandpass filtering (HES-OS)
- Task 3.3 Multi-pixel astronomy via Focal Plane Arrays (RUG)

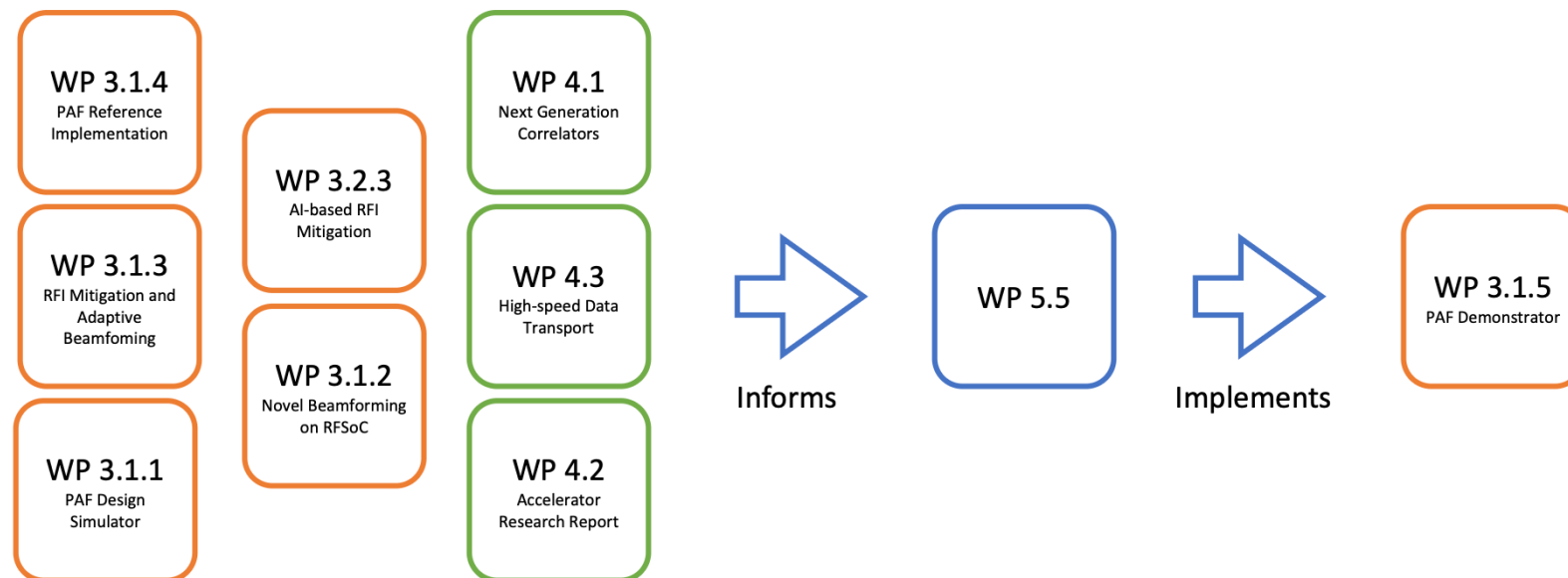


It's all about the people

- All hands meeting
 - 30.03.2023 kick-off
 - 22.09.2023 online
 - 29.01.2024 in person
 - 06.06.2024 in person
 - 07/08.10.2025 in person
- Various Meetings on technical and sub WP level



Interactions within RADIOBLOCKS

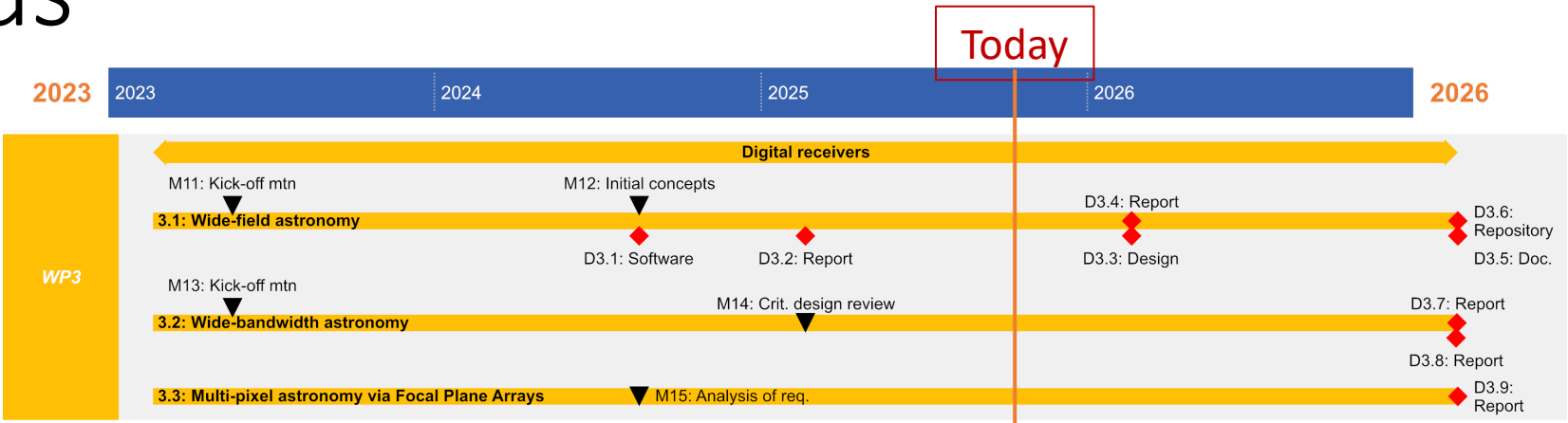


WP3.2.4 /WP2.6 on filter designs

WP3.3 / WP3.1.1 on simulation

...

Status



Number	Description	Due date	Verification	Status
3.1	Kick-off meeting task 3.1	3	Report	✓
3.3	Kick-off meeting task 3.2	3	Report	✓
3.2	Initial beam forming design concepts (task 3.1)	18	Report	✓
3.5	Analysis of requirements (taks 3.3)	18	Report	pending*
3.4	Critical design reviews for DBBC4 and MBRX (task 3.2)	24	Report	pending*

*Milestone 3.5 and 3.4 have been finished but report is not yet formally available. Submission scheduled for Nov 2025



Deliverables

- D3.1: Software (some initial libraries and the setup of the simulation core). These may be written with Matlab, Python or other languages (Task 3.1, month 18) ✓
- D3.2: Report on the simulation work including the development of core modules of the package, all partners to develop similar systems (Task 3.1, month 24) ✓
- D3.3: Design of a scalable digital beamformer based on RFSoc technology suitable for Phased Array Feeds and report on side-by-side performance comparing performance, cost, upgrade path and ease of use with other approaches (Task 3.1, month 36, 28.02.2026)
- D3.4: Report describing the RFI mitigation strategies and their possible ways of being implemented together with their implications on the science data calibration (Task 3.1, month 36, 28.02.2026)
- D3.5: Documentation of the signal processing chain algorithms implemented, including their theoretical backgrounds demonstrated at a successful PAF. (Task 3.1, month 48)
- D3.6: A repository containing all generated software and documentation from the project. (Task 3.1, month 48)
- D3.7: Report on the design and performance DBBC4 VLBI backend prototype (Task 3.2, month 48)
- D3.8: Report on the performance of the implemented wide-band digitizing in the HES-SO MBRX receiver (Task 3.2, month 48)
- D3.9: Report on the potential use of FPAs at high-frequencies. (Task 3.3, month 48)



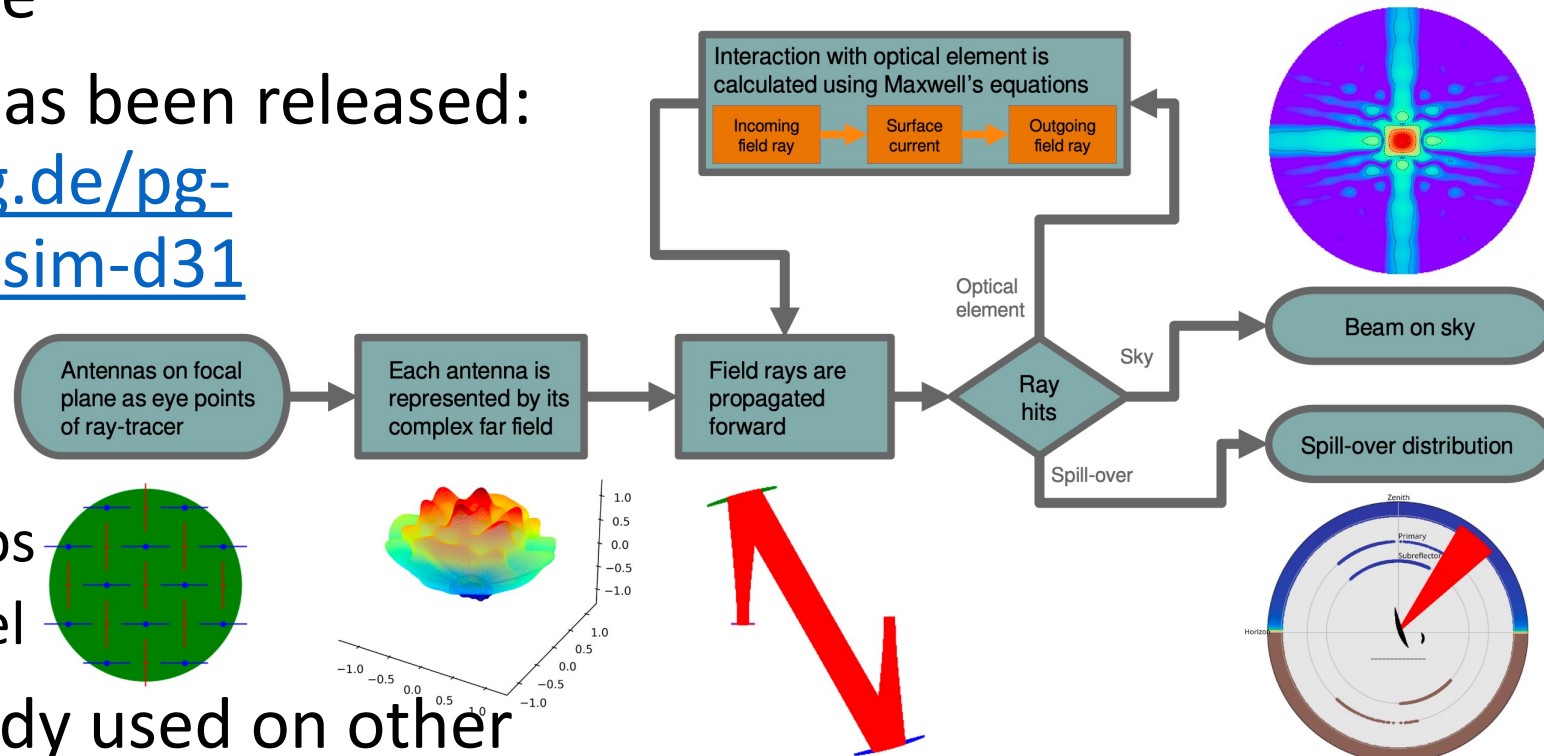
Project Risk

- Available skilled staffing
 - UniMAN and HES-SO were suffering from staff loss
- Delay of cryoPAF availability
- Hardware availability
 - long lead times (low)
 - replacement units (if needed)
- Shipment delays due to export control
- Significant number of deliveries at month 48.

Technical Activities in WP 3.1.1

Design Simulator

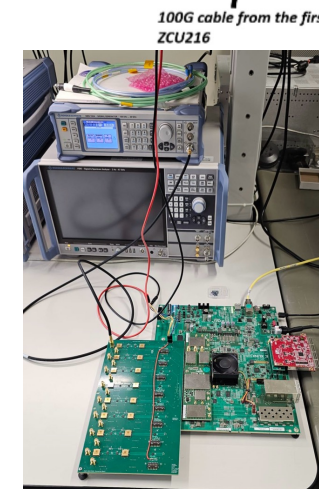
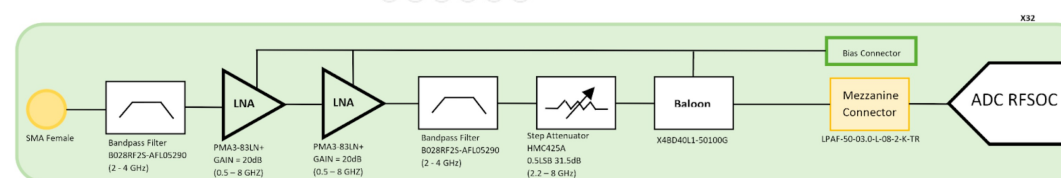
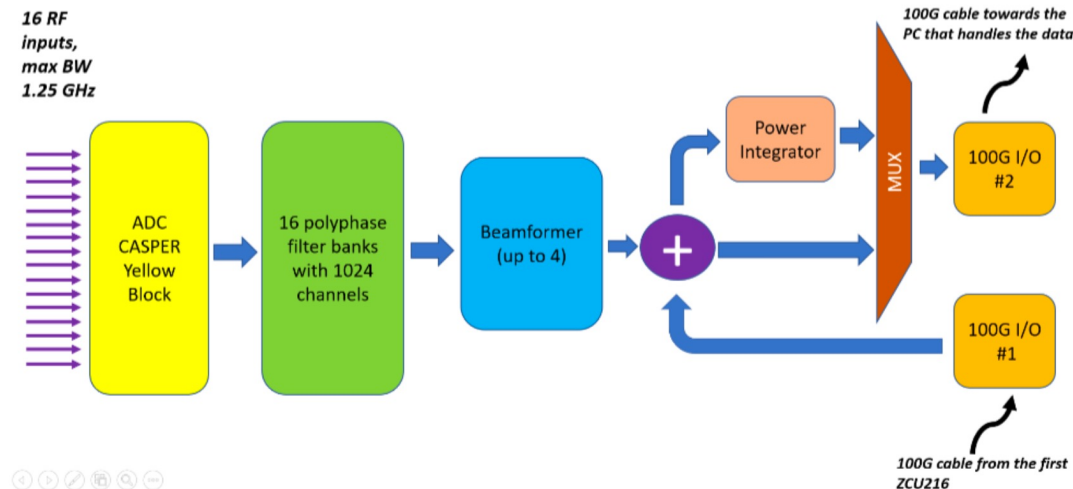
- Focus on maturity of code
- Code + Documentation has been released:
<https://gitlab.mpcdf.mpg.de/pg-radioblocks/paffrontendsim-d31>
- Improvements:
 - Support for GRASP files
 - Custom parameter sweeps
 - Improved spill-over model
- Simulator has been already used on other projects and will be used within WP3.3



Technical Activities in WP 3.1.2

RFSoc-based digital beamformer

- *Design a 32 elements beamformer on RFSoc technology and compare FPGA-only performance with FPGA + GPUs solutions.*
- Using Xilinx Evaluation Kit ZCU216
- *Developments*
 - 100G Mezzanine board
 - CASPERized by Mitch Burnett
 - S-BAND MEZZANINE BOARD DESIGN
 - Operating Band 2.6-3.9 GHz
 - Debug Version fully evaluated
 - Final Version available in 2025
 - Firmware
 - Single board finalized
 - Dual board in progress
- Integrated tests awaiting hardware delivery
- Tests at Effelsberg depends on CryoPAF availability

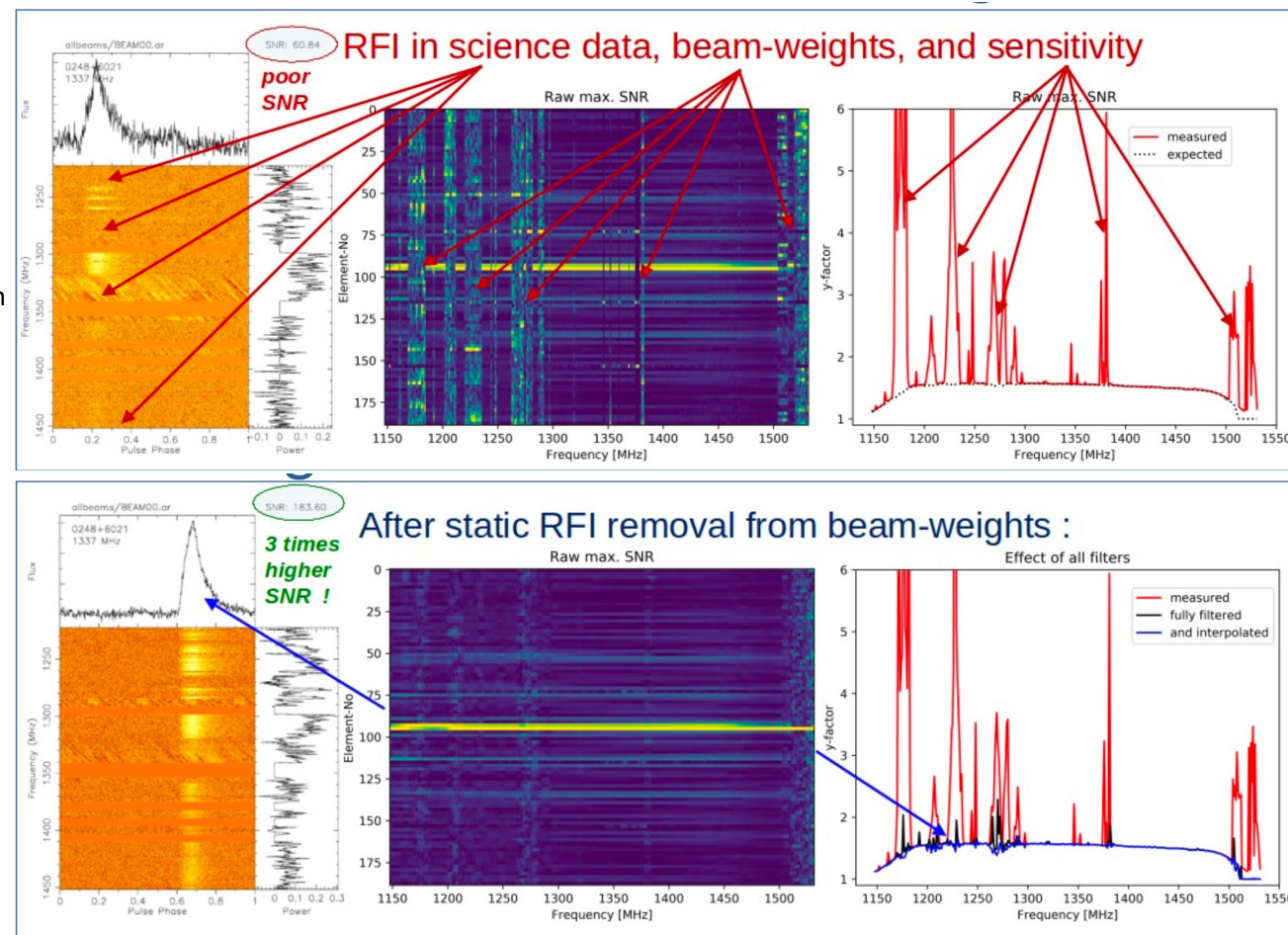


Technical Activities in WP 3.1.3

PAF-RFI mitigation

Derive the capability of a given PAF layout to deal with RFI

- Evaluation of filtering methods
 - Amplitude filtering
 - Using the eigenvector decomposition of R_{on} and R_{off}
 - Spatial filtering
 - Selecting the “right” eigenvector from $R_{on}R_{off}^{-1}$
 - Interpolating over still RFI “empty” section
 - Combining the filters very efficient
- Further evaluation of Algorithmus tests requires new datasets, e.g. from cryoPAF
- D3.4 will be based on the current status



Technical Activities in WP 3.1.4

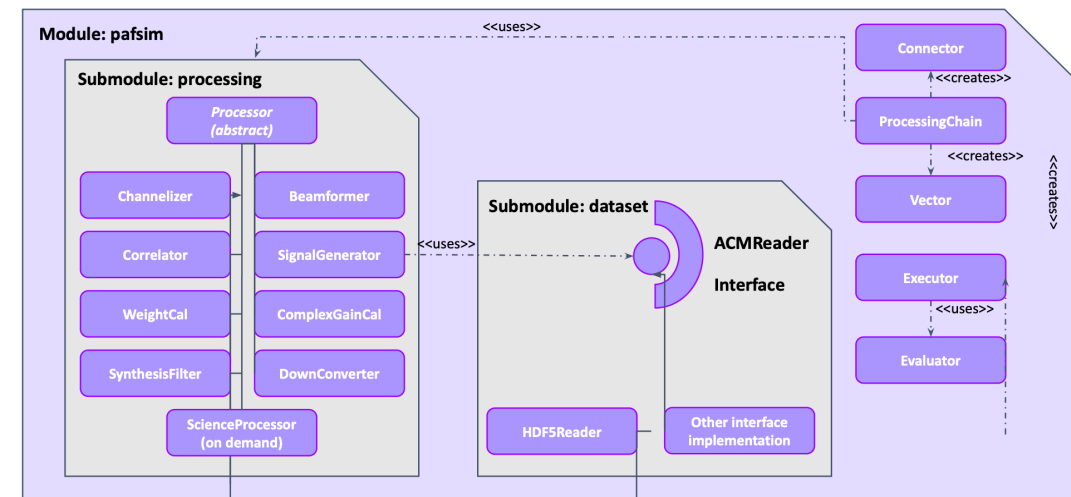
PAF Reference implementation

- Simulator for trialling new algorithms and techniques (e.g. adaptive beamforming, RFI mitigation)
- Testing of realised PAF implementations against the simulator
- Develop a “gold standard” sign
- al processing reference implementation for a PAF
- Development of data quality metric

Code + Documentation has been released:

<https://gitlab.mpcdf.mpg.de/nesser/pafsimCurrentDevelopments>

- Current developments
 - Wideband signal generator
 - Enable validation of the PAF simulator’s capabilities and performance
 - Interface with the PAF frontend simulator
 - A structured container (HDF5) for array correlation matrices (ACM) and simulation metadata
 - Wideband ACM generation
 - Round trip verification
- Future work
 - Extend signal generation:
 - Support more signal varieties and modalities
 - Support standardized output data formats (.npy, .dada, .hdf5)
 - Large data sets, scalability and performance improvements
 - Extended documentation and deliverable report

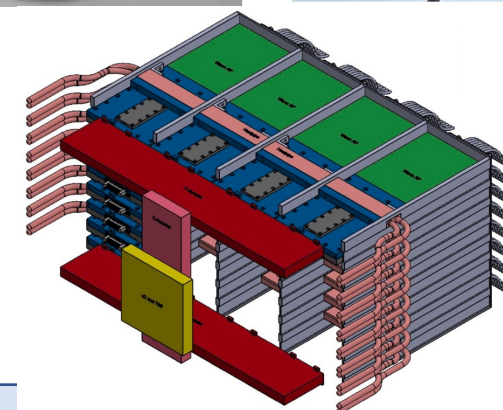
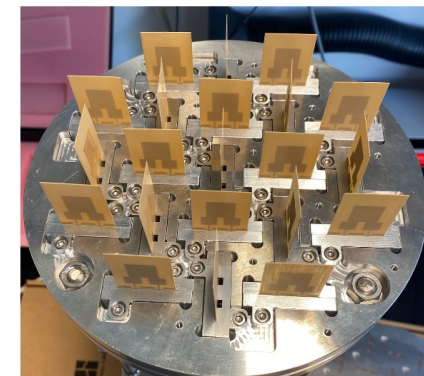
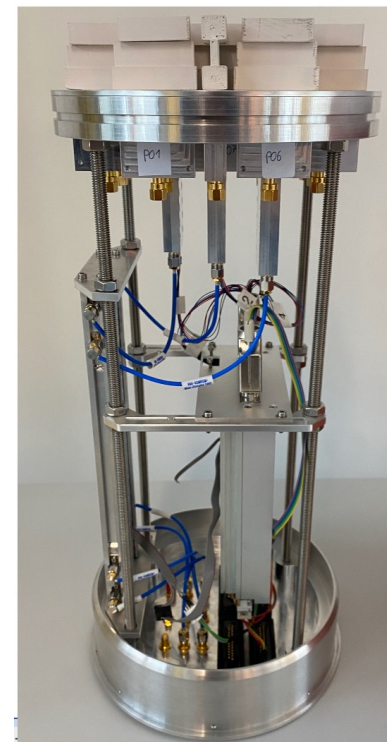


Item	Description	State
Module Architecture	Architecture of the python module (based on UML)	Done (reiterate)
Repository / Dev. Infrastructure	Creation of the Git repository containing software, automated code documentation, CI-pipeline	Done
Documentation	Code documentation, background, reports, results	In progress
Implementation	Basic PAF components and algorithms	Done (reiterate)
	Rudimentary simulated PAF frontend (stand alone)	Replaced
	Interface to WP 3.1.1 (PAF frontend simulation)	done
	Wideband signal generator	done
	Unit tests	done
	Data quality metric, classifier	pending
	Large data sets, scalability and performance improvements	pending



Technical Activities in WP 3.1.5 Demonstrator

- Work on the Demonstrator is ongoing
- Interface towards WP 3.1.2 is defined
- modifications for Radioblocks are identified and mostly implemented already
- Current Status
 - Backend system EDGAR is nearly ready and already partially up and running
 - Channelizer system is progressing and the first units are in Effelsberg already
 - Frontend is still having design issues related to the antenna array
 - Intermediate development of a small PAE operating at ambient temperatures and test it at the Effelsberg 4m dish actually.
 - ADC and signal processing part is evolving fast





Technical Activities WP 3.2

- 100GComo Analogue Conditioning Module
 - Design and construction is finished.
 - Two units have been produced.
 - Integration into test-bed system is done.
- ADCore4
 - Design and construction is finished.
 - Two units have been produced.
 - Integration into test-bed system is done.
- Digital frontend/sampling components
 - DiFrEnd28: Design and construction of is finished. Two units have been produced. Lab testing is ongoing.
 - DiFrEnd4T: Design and construction is is finished. Two units have been produced. Lab testing is ongoing.

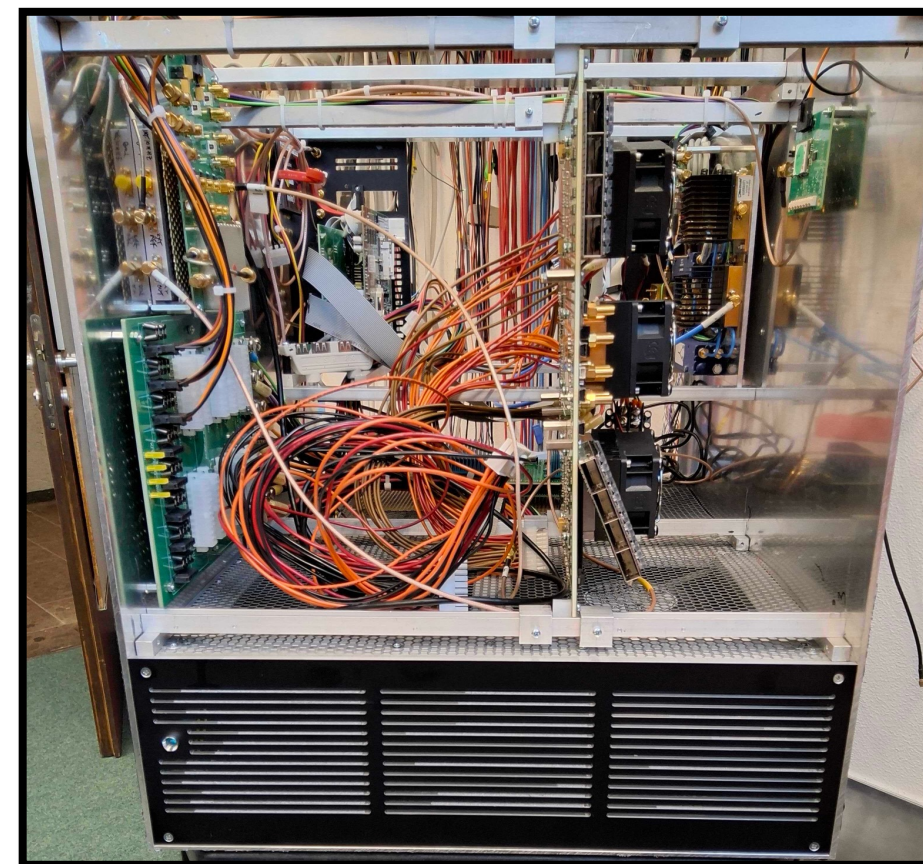
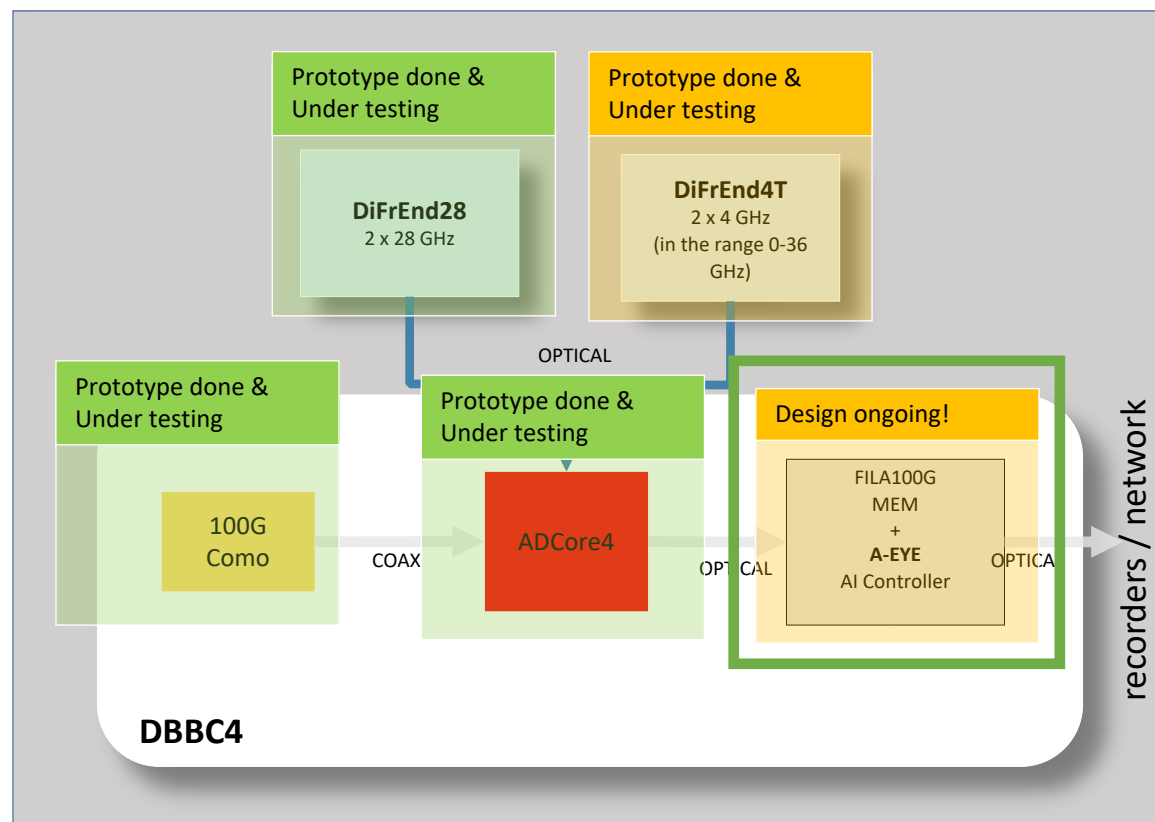


Technical Activities in WP 3.2

- A-EYE / FILA100G components
 - A design change to the original plan has been made. Instead of two separate components the functionality of the two units will be realized with a single multi-purpose board. The new board is an evolution of an FPGA board that was developed as part of the BRAND receiver project. The board will be equipped with interfaces that allow connecting mezzanine boards with dedicated functionality (e.g. fast buffering for the FILA100G use case).
 - The design for the new board is currently ongoing
 - Algorithms for RFI mitigation under development
 - FPGA firmware to be developed
 - The design of the mezzanine boards is pending
 - First tests for the fast memory buffer were carried out. Datarates of 1 Tbps in burst mode (max. 8 seconds) and 56 Gbps in sustained recording mode could be achieved.

Technical Activities in WP 3.2

The integration of the various components into the DBBC4 test-bed has started.



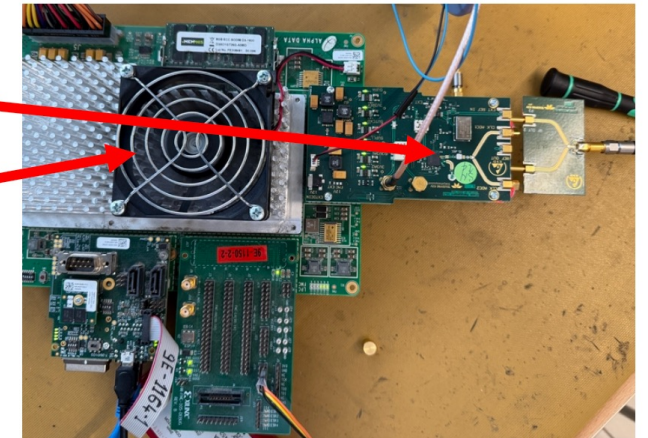
Technical Activities in WP 3.2.3

- **High-frequency characterisation of EV10AS940 and analog**
 - AS940-based digitizer (non-ITAR!) has been characterised to spec
 - Real mode and I/Q DDC, full SW control through SPI/FPGA
 - ADC 1-40GHz 5ENOB@40GHz, low-power analog chain 13-26GHz 15-75dB gain
- **Bandpass filter characterisation**
 - SW-driven Bandpass anti-alias filter for AS940-based digitizer
 - Characterisation of bandpass in “blind-setting” mode (using micro-meter gauge)
 - Goal: for several pass-band characteristics (10...20), characterise the transfer function error

Designed dual AS940 board in testing/debugging (ADC board below visible PLL)

Xilinx KU060 FPGA board

(design must be modified)





Technical Activities in WP 3.3

- Evaluation the use FPA / PAF on Submm telescope
 - Focus on Alma and AtLAST
- Challenges
 - Limited by the feed spacing $2 \cdot w_0$
 - Calibration
 - Practical limits (e.g. Alma cartridge)
 - Data processing
- Further simulation by using WP3.1 code scheduled

General Comments and Outlook

- Implementation of the project
 - Within WP3 joint teams across Europe have been established and operate very efficiently
 - Task leader are on top of project
 - Strong positive Connectivity between the tasks
 - Connections to other WP of RADIOBLOCKS are established
- On time delivery of the tasks
 - Tasks are closely managed by the task leaders
 - Regular meetings (virtual and in persona)
 - Risk due to the deliverables at the end of the project are mitigated by internal milestones
 - Software deliverables are already available on
- Dissemination
 - Participation at various conferences/workshops
- Upcoming deliverables and milestones are advanced and well underway
 - D3.3: Design of a scalable digital beamformer based on RFSoc technology suitable for Phased Array Feeds and report on side-by-side performance comparing performance, cost, upgrade path and ease of use with other approaches (month 36) **(request to delay to month 48)**
 - D3.4: Report describing the RFI mitigation strategies and their possible ways of being implemented together with their implications on the science data calibration (month 36)