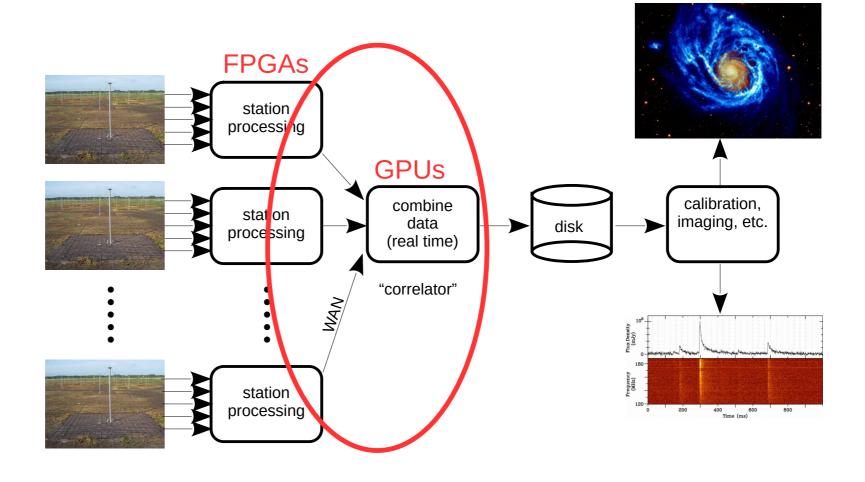
WP4 – Data transport and correlation

John W. Romein, Ilse van Bemmel



WP4: data transport & correlation





Agenda

- recent developments
 - radio blocks (= GPU libraries)
 - data transport
 - correlator / beam-former applications
 - cluster

- planning until end of project
- beyond the project

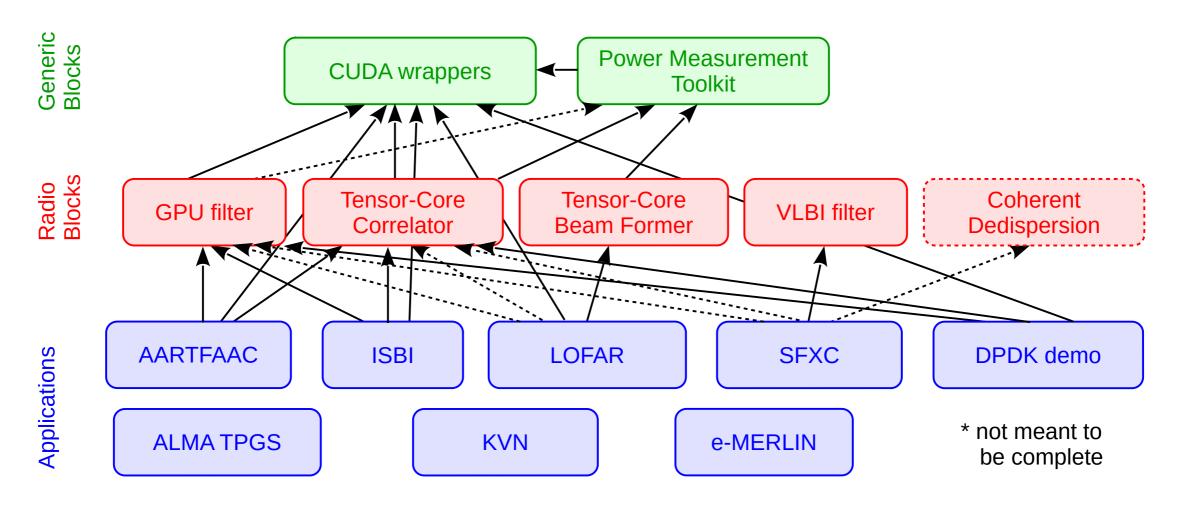


WP4 Goals

- develop common (GPU) "radio blocks" (Task 4.1)
 - code reuse between applications
 - less code maintenance
 - innovative techniques → high (energy) efficiency
- develop/apply methods for 400+ Gb/s FPGA → GPU communication (Task 4.3)
- integrate I/O techniques & radio blocks into correlator / beam-former applications



Generic blocks, radio blocks, and CBF applications

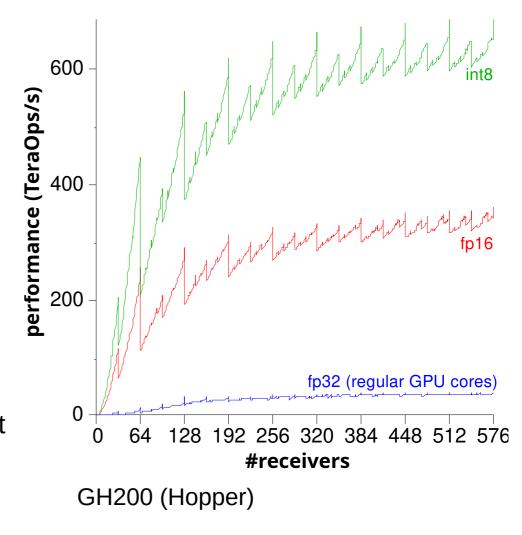




Tensor-Core Correlator

- GPU library for correlations
- uses tensor cores for exceptional performance
- new:

- added Blackwell GPU, fp8, fp4 support
- optimizations \rightarrow ~25% performance improvement

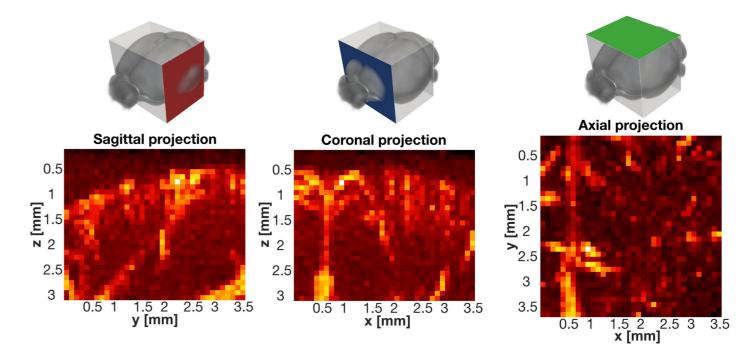






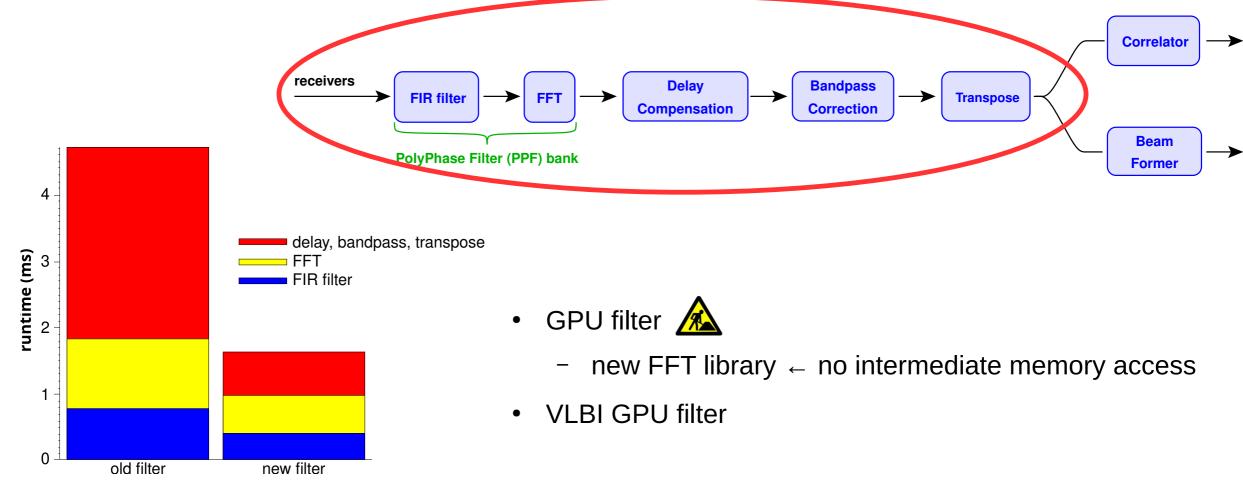
Tensor-Core Beam Former

- new library for beam forming
- uses tensor cores for exceptional performance
- radio astronomy & ultrasound brain imaging
 - fp16, fp8, int1 support
- publication

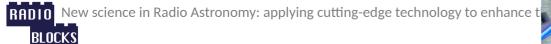




GPU filter libraries



576 recv., 2 pol., 64 channels, 16 taps, 195 kHz, Grace Hopper



Data transport

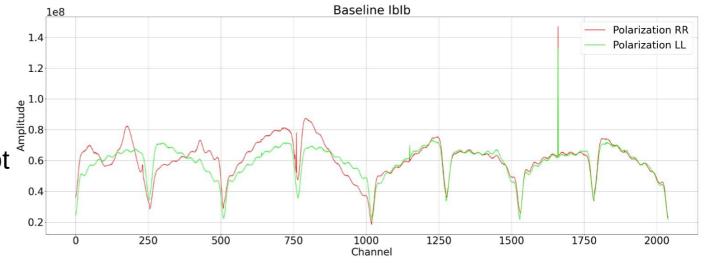


- demonstrated 200 GbE FPGA → CPU
- demonstrated 1.2 Tb/s CPU (mimicking FPGA) → Grace Hopper GPU
 - using Data Plane Development Kit
 - exceptionally fast, but not energy efficient and unhandy \rightarrow exploring alternatives



Correlator applications

- LOFAR (ASTRON):
 - solved performance regression after OS update
 - optimized GPU kernels beam-former pipeline
 - LOFAR 2.0 → removed transpose
- AARTFAAC (ASTRON):
 - already included filter + TCC
 - preparing for 10x bandwidth
- ISBI (VIRAC):
 - ported AARTFAAC correlator
 - bandpass as expected; phases not

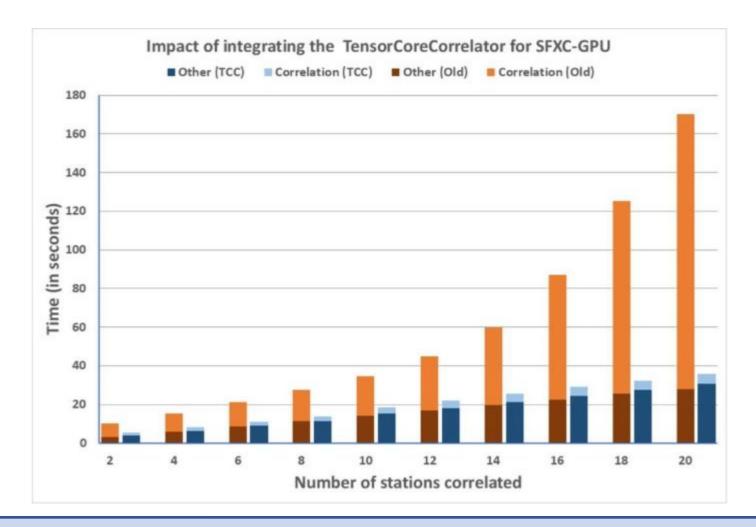


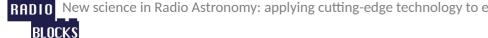


Correlator applications (cntd.)

SFXC (JIVE):

- integrated TCC and VLBI
 GPU filter into SFXC
- e-Merlin (UMan):
 - uses SFXC (CPUs)

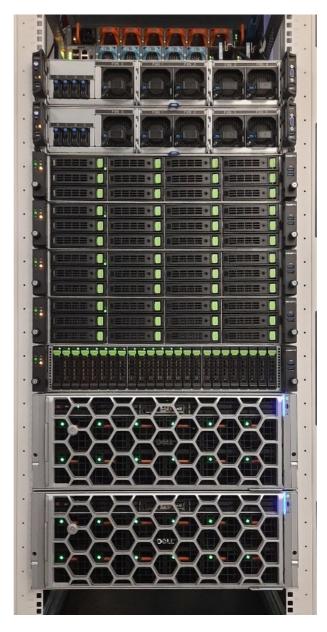






The Radioblocks Cluster

- problematic procurement (complexity, budget, time)
- just delivered and tested
- ordering new-generation **GPUs and NICs**
- also accessible to other WPs



400 GbE switch

Grace Hoppers

GPU nodes

head node (incl. ~200 TB SSD storage)

"fat" GPU nodes (incl. PCIe switches)



Deliverables and Milestones

- 17 (M4.2): Verification of high-speed prototype (Task 4.3, month 18) ✓
- **D4.3**: Prototype high-speed data transport (Task 4.3, month 24) ✓
- **D4.4**: Basic correlator on TensorCore architecture (Task 4.1, month 24) ✓
- 18 (M4.3): Demonstrator benchmark defined (Task 4.1, month 30)



Publications

Christiaan Boerkamp, Steven van der Vlugt, and Zaid Al-Ars. **Tina: Acceleration of Non-NN Signal Processing Algorithms Using NN Accelerators.** *IEEE International Workshop on Machine Learning for Signal Processing (MLSP)*, London, United Kingdom, 2024. Preprint: https://doi.org/10.48550/arXiv.2408.16551

Leon Oostrum, Bram Veenboer, Ronald Rook, Pieter Kruizinga, Michael Brown and John W. Romein. **The Tensor-Core Beam Former:** a High-Speed Signal-Processing Library for Multidisciplinary Use. *IEEE International Parallel and Distributed Processing Symposium (IPDPS'25), Milan, Italy, June 3-7, 2025.* Preprint: https://doi.org/10.48550/arXiv.2505.03269

John W. Romein. Breaking the I/O Barrier: 1.2 Tb/s Ethernet Packet Processing on a GPU. Euro-Par'25, Dresden, Germany, August 25-29, 2025

Steven van der Vlugt, Leon Oostrum, Gijs Schoonderbeek, Ben van Werkhoven, Bram Veenboer, Krijn Doekemeijer and John Romein. **PowerSensor3: A Fast and Accurate Open Source Power Measurement Tool.** *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'25), Ghent, Belgium, May 11-13, 2025.* Preprint: https://doi.org/10.48550/arXiv.2504.17883

Victor Van Wijhe, Vincent Sprave, Daniele Passaretti, Nikolaos Alachiotis, Gerrit Grutzeck, Thilo Pionteck, and Steven v.d. Vlugt. **Exploring the Versal Al Engines for Signal Processing in Radio Astronomy,** 34th International Conference on Field-Programmable Logic and Applications (FPL), Torino, Italy, 2024, pp. 1-10, doi: 10.1109/FPL64840.2024.00011.

+ several workshop presentations



Planning 3rd period

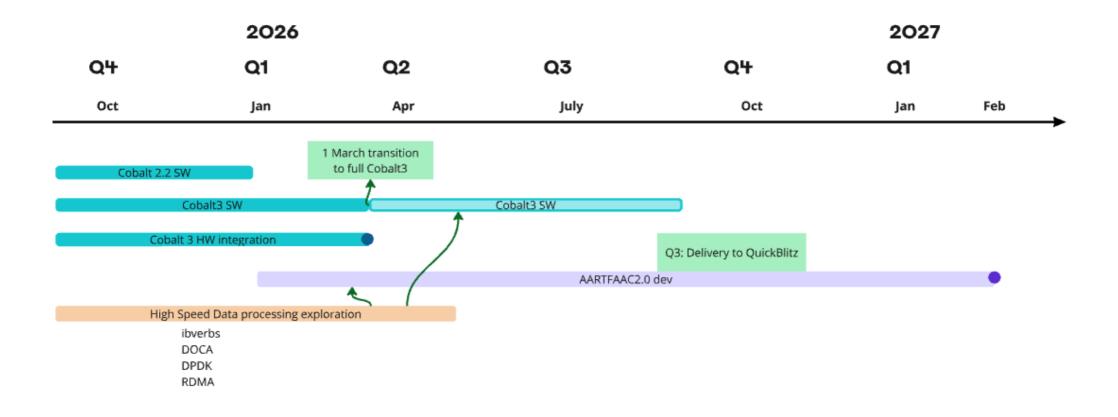
GPU filter → mature

- explore DPDK alternative
- focus shift from radio blocks to applications

ASTRON	LOFAR	prepare for LOFAR 2.0; integrate filter & TCC
	AARTFAAC	adapt input format; prepare for 1.2 Tb/s
ESO, ASTRON	ALMA	correlator study: reduce input handling overhead
JIVE	SFXC	multiple phase centers; coherent beam forming; end-to-end VLBI correlation
UBx	ALMA	digitizer tests: develop 200/400 GbE packet capture application & correlator
UMan	eMerlin	
VIRAC	ISBI	fix phase (delay?) errors; make real time



ASTRON planning





Upcoming deliverables

- **D4.5**: Beamforming and coherent dedispersion modules (Task 4.1, month 36)
- **D4.6**: Next-generation correlator demonstrator (Task 4.1, month 48)



Risks

- hardware purchase (already materialized)
- applications not completed in time



Beyond the project

- GPUs prevail for next 5 years
- need to maintain current software
- ALMA GPU correlator study (ESO)
- GPUs in other parts of processing pipeline
- space



Summary

- radio blocks progressing well
- I/O: fast but not (energy) efficient → studying alternatives
- focus shift to applications